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CLAIMS

1. A method of manufacturing a semiconductor device comprising the steps of:

forming a gate insulation layer on a semiconductor region formed of silicon carbide having a (000-1) face orientation;

forming a gate electrode on the gate insulation layer;

forming an electrode on the semiconductor region; and

cleaning a surface of the semiconductor region

wherein the gate insulation layer is formed in an atmosphere containing 1% or more H₂O (water) vapor at a temperature of from 800°C to 1150°C to reduce an interface trap density of an interface between the gate insulation layer and the semiconductor region.

2. A method according to claim 1, wherein the gate insulation layer is formed in an atmosphere containing H₂O vapor at a temperature of from 800°C to 1050°C.

3. A method of manufacturing a semiconductor device comprising the steps of:

forming a gate insulation layer on a semiconductor region formed of silicon carbide having a (000-1) face orientation;

forming a gate electrode on the gate insulation layer;

forming an electrode on the semiconductor region; and

cleaning a surface of the semiconductor region;

forming a gate insulation layer;

wherein the step of forming the gate insulation layer is followed by heat treatment in an atmosphere containing H₂ (hydrogen) gas or H₂O (water) vapor to reduce an interface trap density of an interface between the gate insulation layer and the semiconductor region.

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4. A method of manufacturing a semiconductor device comprising the steps of:

forming a gate insulation layer on a semiconductor region formed of silicon carbide having a (000-1) face orientation;

forming a gate electrode on the gate insulation layer;

forming an electrode on the semiconductor region; and

cleaning a surface of the semiconductor region;

wherein the step of forming the gate insulation layer is followed by heat treatment in an atmosphere containing H₂O (water) vapor, followed by heat treatment in an atmosphere containing H₂ (hydrogen) gas to reduce an interface trap density of an interface between the gate insulation layer and the semiconductor region.

5. A method according to claim 2 or 3, wherein the heat treatment following the forming of the gate insulation layer is carried out in a mixed gas atmosphere of H₂ (hydrogen) gas and inert gas in which the H₂ (hydrogen) gas has a predetermined concentration of from 1% to 100%.

6. A method according to claim 2 or 3, wherein the heat treatment following the forming of the gate insulation layer is carried out in a mixed gas atmosphere of H₂O (water) vapor and inert gas in which the H₂O (water) vapor has a predetermined concentration of from 1% to 100%.

7. A method according to any one of claims 3, 5 and 6, further comprising a heat treatment step in which the semiconductor region is maintained for a predetermined time in an inert gas atmosphere at a predetermined temperature, between the step of forming a gate insulation layer and the step of heat treatment in an atmosphere containing H₂ (hydrogen) gas or H₂O (water) vapor.

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8. A method according to any one of claims 4 to 6, further comprising a heat treatment step in which the semiconductor region is maintained for a predetermined time in an inert gas atmosphere at a predetermined temperature, in a first period between the step of forming a gate insulation layer and the step of heat treatment in an atmosphere containing H_2O (water) vapor, or in a second period between a heat treatment step in an atmosphere containing H_2O (water) vapor and a heat treatment step in an atmosphere containing H_2 (hydrogen) gas.
9. A method according to any one of claims 4 to 6 and 8, wherein the heat treatment in an atmosphere containing H_2O vapor takes place at a higher temperature than the heat treatment in an atmosphere containing H_2 gas.
10. A method according to any one of claims 3 to 9, wherein the step of heat treatment in an atmosphere containing H_2O (water) vapor, following the step of forming a gate insulation layer, is maintained for a predetermined time at a predetermined temperature of from 650°C to 950°C .
11. A method according to any one of claims 3 to 10, wherein the gate insulation layer is formed by thermal oxidation of the semiconductor region.
12. A method according to claim 11, wherein the thermal oxidation of the semiconductor region is carried out in an atmosphere containing H_2O (water) vapor.
13. A method according to claim 12, wherein the atmosphere containing H_2O vapor comprises H_2O vapor and oxygen, or H_2O vapor,

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oxygen and inert gas, in which the H_2O gas has a predetermined concentration of from 1% to 100%.

14. A method according to claim 13, wherein when the heat treatment following the forming of the gate insulation layer is carried out in an atmosphere containing H_2O vapor that comprises H_2O vapor and oxygen gas, or H_2O vapor, oxygen and inert gas, in which the H_2O vapor has a predetermined concentration of from 10% to 50%.

15. A method according to any one of claims 1 to 14, wherein the H_2O (water) vapor is produced by a reaction between hydrogen (H_2) gas and oxygen (O_2) gas in the atmosphere in which the semiconductor region is placed.

16. A method according to claim 15, wherein a ratio $[\text{O}_2]/[\text{H}_2]$ between a flow rate $[\text{H}_2]$ of H_2 (hydrogen) gas and a flow rate $[\text{O}_2]$ of O_2 (oxygen) gas is within a predetermined range of from 0.1 to 100.

17. A method according to any of claims 3 to 16, wherein a semiconductor region oxidation temperature is within a predetermined range of from 800°C to 1150°C .

18. A method according to any one of claims 11 to 17, wherein when the heat treatment following the forming of the gate insulation layer by thermal oxidation of the semiconductor region is carried out in an atmosphere containing H_2O vapor, the heat treatment is carried out at a temperature that is lower than a temperature at which the gate insulation layer is formed to increase a thickness of the gate oxide layer without increase of a thickness of the gate oxide layer.

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19. A method according to any one of claims 3 to 18, wherein the heat treatment in an atmosphere containing H_2 (hydrogen) gas is carried out at a temperature within a predetermined range of from $600^{\circ}C$ to $900^{\circ}C$.

20. A method according to any one of claims 3 to 19, wherein formation of the gate insulation layer and the following heat treatment in an atmosphere of H_2 (hydrogen) gas, H_2O (water) vapor or inert gas are carried out as a continuous process inside an apparatus shut off from outside air.

21. A method according to any one of claims 1 to 20, wherein the step of cleaning the surface of the semiconductor region uses ultraviolet irradiation to clean the semiconductor region placed in an ozone atmosphere.

22. A method according to any one of claims 1 to 21, wherein the step of cleaning the surface of the semiconductor region uses heat treatment in a H_2 (hydrogen) gas atmosphere.

23. A method according to claim 22, wherein the step of cleaning the surface of the semiconductor region includes a step of using ultraviolet irradiation to clean the semiconductor region placed in an ozone atmosphere, followed by a step of cleaning using heat treatment in a H_2 (hydrogen) gas atmosphere.

24. A method according to any one of claims 1 to 23, further comprising the steps of forming an interlayer insulation layer, forming a wiring layer and forming an insulation layer that protects the wiring layer.

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25. A method according to any one of claims 3 to 24, wherein the heat treatment in an atmosphere containing H_2 gas is carried out after forming a gate electrode layer above the gate insulation layer.

26. A method according to any of claims 3 to 25, further comprising a step of heat treatment in an atmosphere containing H_2 (hydrogen) gas followed by a step of heat treatment in an inert gas atmosphere at up to $600^\circ C$.

27. A semiconductor device comprising a gate insulation layer on a semiconductor region of (000-1) face silicon carbide, a gate electrode on the gate insulation layer and an electrode on the semiconductor region, wherein a hydrogen or hydroxyl group (OH) level in the gate insulation layer is from $1E19/cm^3$ to $1E20/cm^3$.

28. A semiconductor device according to claim 27, wherein the semiconductor device is a metal-insulator-semiconductor (MIS) field effect transistor (FET) or a MIS capacitor.

29. A semiconductor device according to claim 28, wherein the MISFET is an n-channel type.

30. A semiconductor device according to claim 28, wherein the MISFET is a p-channel type.

31. A semiconductor device according to claim 27, wherein the semiconductor device is a circuit having a complementary metal-insulator-semiconductor (CMIS) composed of the MISFET or MIS capacitor according to claims 29 and 30.

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32. A semiconductor device according to claim 27, wherein the semiconductor device is a lateral resurf metal-insulator- semiconductor field effect transistor (lateral resurf MISFET) or a lateral double MIS field effect transistor (lateral DMISFET).

33. A semiconductor device according to claim 27, wherein the semiconductor device is a vertical DMISFET.

34. A semiconductor device according to claim 27, wherein the semiconductor device is an insulated gate bipolar transistor (IGBT).

35. A semiconductor device according to claim 34, wherein the semiconductor device is a p-channel IGBT.

36. A semiconductor device comprising a gate insulation layer on a semiconductor region of (000-1) face silicon carbide, a gate electrode on the gate insulation layer and an electrode on the semiconductor region, wherein a hydrogen or hydroxyl group (OH) level at an interface between the gate insulation layer and the semiconductor region is within a range of from $1\text{E}20/\text{cm}^3$ to $1\text{E}22/\text{cm}^3$.

37. A semiconductor device according to claim 36, wherein the semiconductor device is a MISFET or a MIS capacitor.

38. A semiconductor device according to claim 37, wherein the MISFET is an n-channel MISFET.

39. A semiconductor device according to claim 37, wherein the MISFET is a p-channel MISFET.

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40. A semiconductor device according to claim 36, wherein the semiconductor device is a circuit having a CMIS comprising the MISFET or MIS capacitor according to claims 38 and 39.

41. A semiconductor device according to claim 36, wherein the semiconductor device is a lateral resurf MISFET or lateral DMISFET.

42. A semiconductor device according to claim 36, wherein the semiconductor device is a vertical DMISFET.

43. A semiconductor device according to claim 36, wherein the semiconductor device is an IGBT.

44. A semiconductor device according to claim 43, wherein the semiconductor device is a p-channel IGBT.